WHAT IS CLAIMED IS:

Sub A1

1. An image processor comprising:

a plurality of processors processing input image data in parallel with each other and outputting processed said image data; and

an address memory storing address information of said image data processed by each of said plurality of processors.

2. The image processor in accordance with claim 1, further comprising:

an image memory storing said image data output from said plurality of processors, and

read means reading said image data from said image memory on the basis of said address information stored in said address memory.

3. The image processor in accordance with claim 1, further comprising an image memory storing said image data output from said plurality of processors along the sequence of addresses on the basis of said address information stored in said address memory.

4. The image processor in accordance with claim 1, further comprising:

input means inputting image data subjected to processing in synchronization with a first external device, and

output means outputting said image data processed in said plurality of processors and said address information stored in said address memory in synchronization with a second external device.

5. The image processor in accordance with claim 1, wherein said plurality of processors also output arrangement information corresponding to processed said data when outputting said data.

6. An image processor comprising:

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a plurality of processors performing prescribed processing on a plurality of data divided from single image data respectively;

a first memory storing arrangement information in original image data for said plurality of divided data; and

a controller restoring a single image from said plurality of data processed in said plurality of processors in accordance with said arrangement information.

7. The image processor in accordance with claim 6, further including a second memory storing said data processed in said plurality of processors, wherein said controller reads said data from said second memory in sequence along said arrangement information and restores said image.

8. The image processor in accordance with claim 6, further including an image memory, wherein said controller stores processed said data in positions of said image memory corresponding to said arrangement information.

9. The image processor in accordance with claim 6, wherein said first memory is provided in correspondence to each of said plurality of processors.

10. The image processor in accordance with claim 9, wherein said plurality of processors also output arrangement information corresponding to processed said data when outputting said data.

11. An image processing method including steps of:

dividing input image data into a plurality of image data;

performing image processing on said divided image data with a plurality of processors;

outputting said processed data as well as address information indicating arrangement of said divided data; and

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restoring a single image from said processed data in accordance with said address information.